IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hang-Dony Kuan, et al. **Art Unit: 2829**

Serial No.: 10/804,374 **Examiner: Arleen M. Vazquez**

Filed: 03/19/04 **Docket: TI-36952**

For: IC TESTING APPARATUS AND METHODS

APPELLANTS' BRIEF UNDER 37 C.F.R. §1.192

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed January 23, 2006. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

Claims 6-8, 10, and 11 are the subject of this appeal. Claims 6-8, 10, and 11 are rejected. This application was filed on March 19, 2004.

STATUS OF THE AMENDMENTS

The Appellants filed an amendment under 37 C.F.R. § 1.116 on March 17, 2006 in response to the Office Action dated January 23, 2006, with no amendments to the claims. The Appellants filed an amendment under 37 C.F.R. § 1.111 on December 28, 2005 in response to the Office Action dated November 7, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

First referring primarily to Figure 1, an overview of examples of preferred embodiments of methods, systems, and apparatus of the invention is provided. A DUT 10 is shown. The DUT 10 may be a packaged semiconductor device, such as a surface-mount BGA, for example. The DUT 10 is preferably mounted in a socket 12. The socket 12 is positioned on a PCB test board 16 designed to interface with automatic test equipment (ATE) 18. Further referring to Figure 2, a close-up partial cross-section is shown. The DUT 10 has a contact surface 20, in this case a bond pad 20 with a solder ball 22 attached. A test probe, in this instance a pogo pin 24, extends from the upper surface 26 of the socket 12 to the lower surface 28. The pin 24 functions as an electrical path between the DUT 10 and the test board 16. As shown, the upper tip 30 of the pin 24 contacts the solder ball 22. It is known that the solder ball 22 is relatively soft metal such as a mixture of various amounts of lead, tin, and silver. As a result, the solder ball 22 has a tendency to conform somewhat to the upper tip 30 of the pin. Thus, the contact between the solder ball 22 and the top 30 of the pin 24 is generally sufficient in area and firmness in order to provide a reliable electrical path.

At the opposing end 32 of the pin 24, contact 34 is made with a contact area 36 on the test board 16. The contact area 36 is typically metal, often multiple layers, including copper, nickel, or gold. The contact area 36 has a probe or pin receptacle 38 for receiving the bottom tip 32 of the pin 24 in order to ensure staunch electrical contact

34 between the pin 24 and the contact area 36 on the test board 16. The total area of contact 34 is increased by the correspondence of the pin tip 32 and the pin receptacle 38. The contact area 36 of the test board 16 is connected to the ATE (not shown) for making test measurements as is common in the arts. The electrical path between the DUT 10 and the ATE includes the staunch contact 34 between the pin 24 and pin receptacle 38 through which accurate measurements may be made. It has been found that a superior electrical path is provided using the receptacle 38 and pin 24 arrangement, particularly when operating at the high frequencies of modern RF devices.

Now referring primarily to Figure 3, another example of preferred embodiments of the invention is shown beginning with a cross section view of a portion of a partially assembled test board 16. The PCB 16 includes a top layer 40, which may be a layer of insulating material. The board 16 also has contact areas 36 used for making electrical connections externally to a DUT and ATE. The contact areas 36 are electrically connected to other layers 44 or portions of the test board 16 internally or to ground (not shown). Typically vias 37 are used to make electrical connections among layers of the PCB 16, such as between a contact area 36 at the surface and one or more subsurface layer 44. Generally, a test board 16 has numerous contact areas 36 designed to make the ATE operative when coupled to various external inputs and outputs of a DUT (not shown).

Now referring primarily to Figure 6, a partial cross section showing an example of an embodiment of a test board 16 constructed according to the invention is illustrated. The test board 16 shown may be constructed with a receptacle 38 by layering as described. Alternatively, a test board 16 with a completed contact area 36 may be drilled using precision drilling equipment to form a receptacle 38. A test probe, or pin 24, inserted into the pin receptacle 38 of a multilayer contact area 36 is shown. The test pin 24 is preferably generally conical or hemispherical at its lower tip 32 in order to facilitate substantial areas of firm contact 34 between the surface of the pin receptacle 38 and the tip 32 of the test pin 24.

Understanding of the invention may be enhanced by reference to Figure 7, which shows a top view of the test board 16 of Figure 6 with the pin 24 cut away at line 7-7. The pin 24 may be seen inserted into the receptacle 38 of the contact area 36 for making firm electrical contact between the test board 16 and the pin 24, which through the conductor-filled via 37, is in turn electrically connected to the ATE and DUT (not shown).

An alternative embodiment of the invention, is shown in Figures 8-12, demonstrating that a pin receptacle 38 may be formed atop a via 37 on the test board 16. As shown in Figure 8, a cross section view of a portion of a partially assembled test board 16, the PCB 16 includes a top layer 40 of non-conducting material. The board 16 also has contact areas 36 used for making electrical connections externally to a DUT

and ATE. The contact areas 36 are electrically connected to other layers 44 or portions of the test board 16 internally or to ground (not shown). A via 37 is used to form electrical connections among two or more layers of the PCB 16, such as between a contact area 36 at the surface and one or more subsurface layer 44. Referring to Figure 9, the contact area 36 is shown overlain by a first metal layer 46. The first metal layer 46 is formed to define a contact area 36, preferably more or less centered on the via 37. The first metal layer 46 is preferably deposited within the via 37 as well. A second metal layer 50 is preferably formed atop the first metal layer 46, as depicted in Figure 10, covering the contact area and substantially filling the via 37.

Now referring primarily to Figure 11, a partial cross section showing an example of an embodiment of a test board 16 constructed according to the invention is illustrated with a test pin 24 inserted into the pin receptacle 38 of a multilayer contact area 36 is shown. The test pin 24 is preferably generally conical or hemispherical at its lower tip 32 in order to facilitate substantial areas of firm contact 34 between the surface of the pin receptacle 38 and the tip 32 of the test pin 24.

An alternative view of the invention appears in Figure 12, showing a partial cut-away top view of the test board 16 according to the embodiment of the invention shown in Figure 11 with the pin 24 cut away at line 12-12. The pin 24 is shown inserted into the receptacle 38 of the contact area 36 for making firm electrical contact between the test board 16 and the pin 24. The pin 24, through the conductor-filled via 37, is in turn

electrically connected to the ATE and DUT (not shown).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Rejection under 35 U.S.C. § 102 (e) as being anticipated by US Patent No. 6,856,154.

ARGUMENT

Rejection under 35 U.S.C. § 102 (e) as being anticipated by US Patent No. 6,856,154

Claims 6-8, 10, and 11

Claim 6 includes **"**...a socket for receiving a DUT, the socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board; the test board adjoining the socket, the test board having pin

receptacles for receiving the opposing ends of the pins ...". The references of record do not show, teach, or suggest the above limitations of claim 6. Board 320 in Song is not connected to board 400 by pin receptacles for receiving the opposing ends of pins, it is connected by wire cables 340 (see column 4, lines 52 and 53). The Song reference also does not disclose a socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board. The contact with board 320 in Song is with wire cables 340.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 6-8, 10 and 11 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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CLAIMS APPENDIX

6. A system for testing a singulated semiconductor device (DUT) comprising:

a socket for receiving a DUT, the socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board;

the test board adjoining the socket, the test board having pin receptacles for receiving the opposing ends of the pins; and

measuring means operably coupled to the test board pin receptacles for measuring electrical signals in the DUT.

7. A system according to claim 6 wherein the receptacles each further comprise a basin for receiving the pin.

8. A system according to claim 6 wherein the receptacles each further comprise a generally conical basin for receiving the pin.

10. A system according to claim 6 wherein the receptacles each further comprise a precision drilled basin.

11. A system according to claim 6 wherein the receptacles each further comprise an etched basin.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.